

FIG. 1

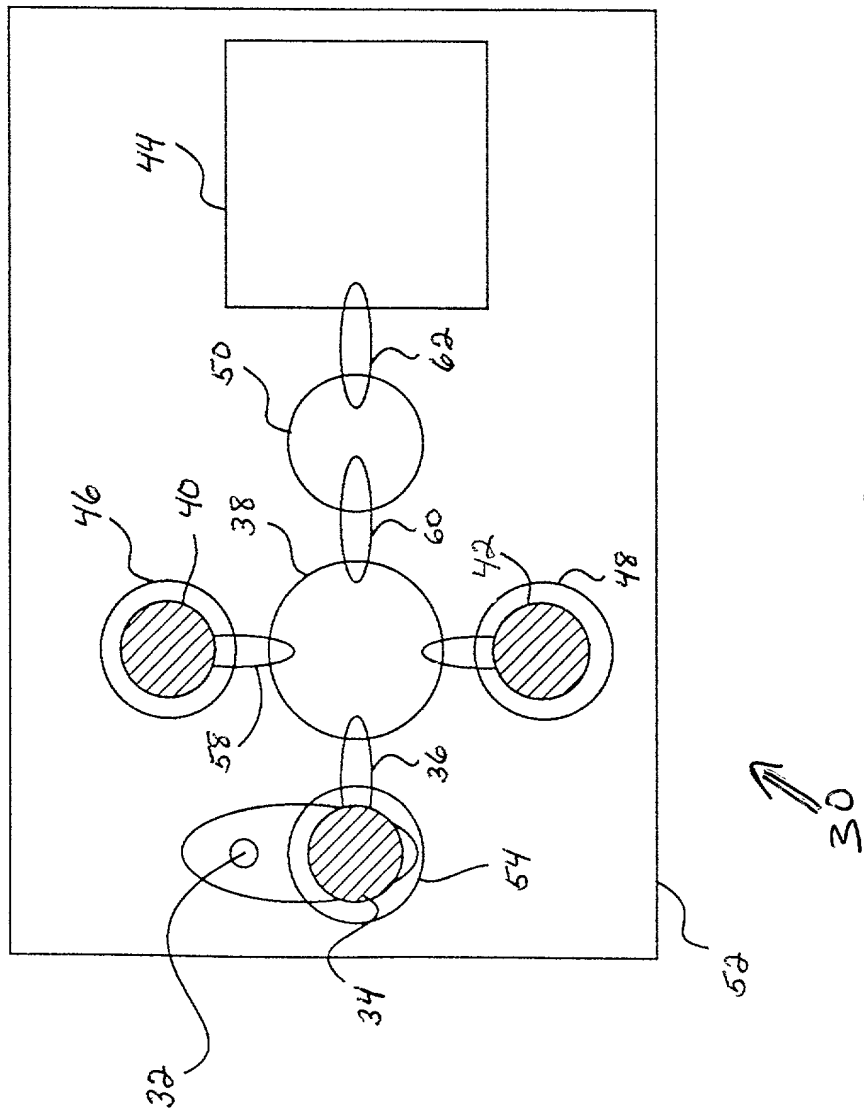


FIG. 2

FIG. 2A is a schematic diagram of a device 100 in a first state. The device 100 includes a substrate 110, a gate stack 120, a source/drain region 130, and a channel region 140. The gate stack 120 is disposed on the substrate 110 and includes a gate dielectric layer 121 and a gate electrode layer 122. The source/drain region 130 is disposed on the substrate 110 and includes a source/drain dielectric layer 131 and a source/drain electrode layer 132. The channel region 140 is disposed on the substrate 110 and includes a channel dielectric layer 141 and a channel electrode layer 142. The device 100 is configured to operate in a first state, in which the gate electrode layer 122 is electrically coupled to the source/drain electrode layer 132 and the channel electrode layer 142.

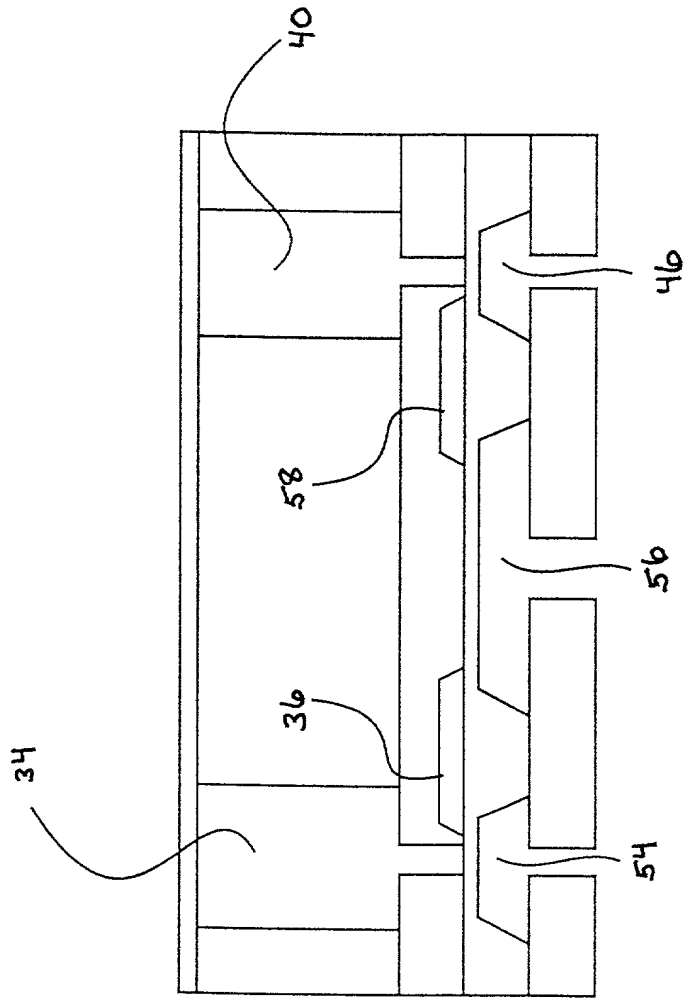
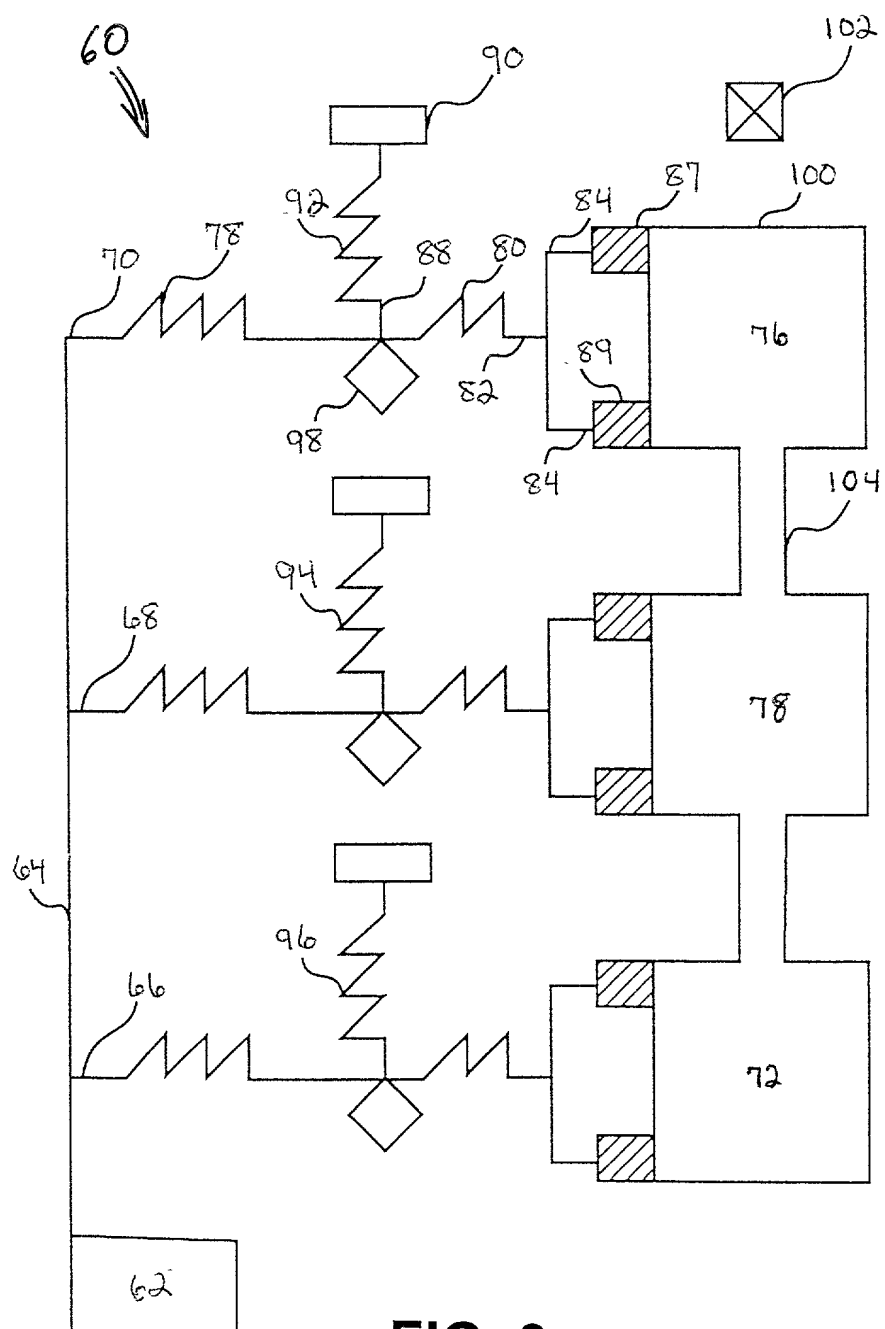
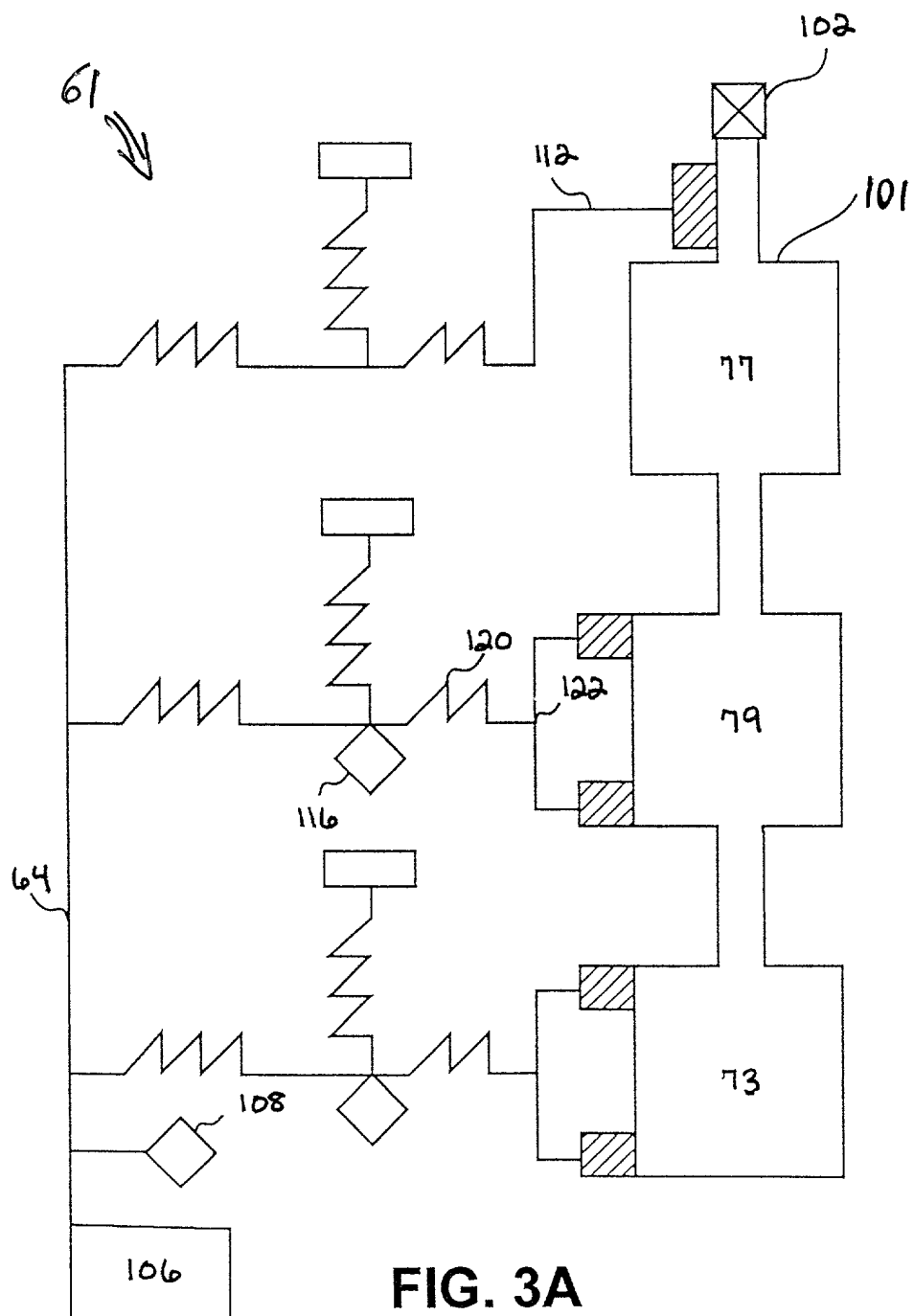
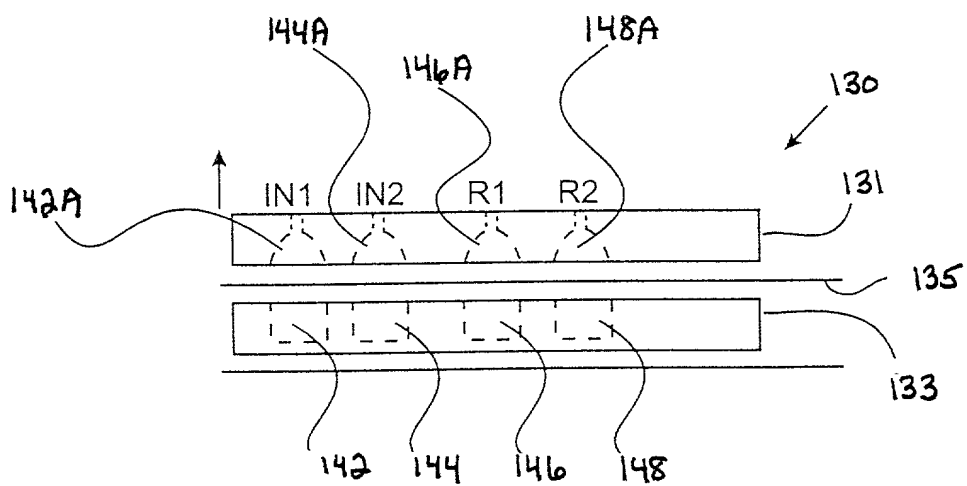


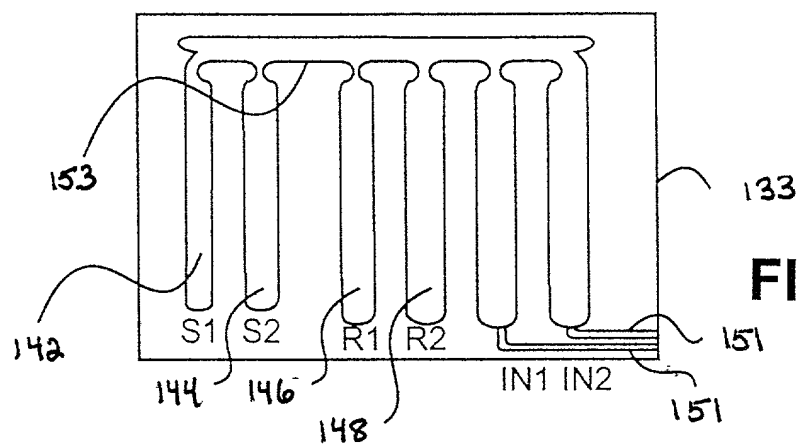
FIG. 2A



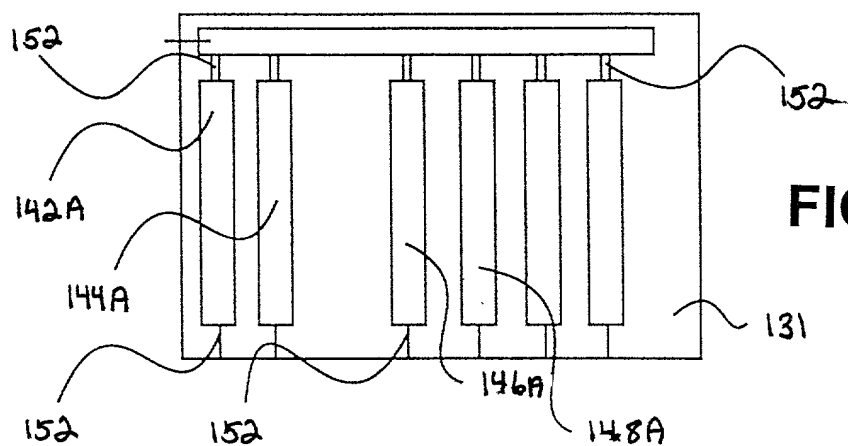




**FIG. 4**



**FIG. 4A**



**FIG. 4B**

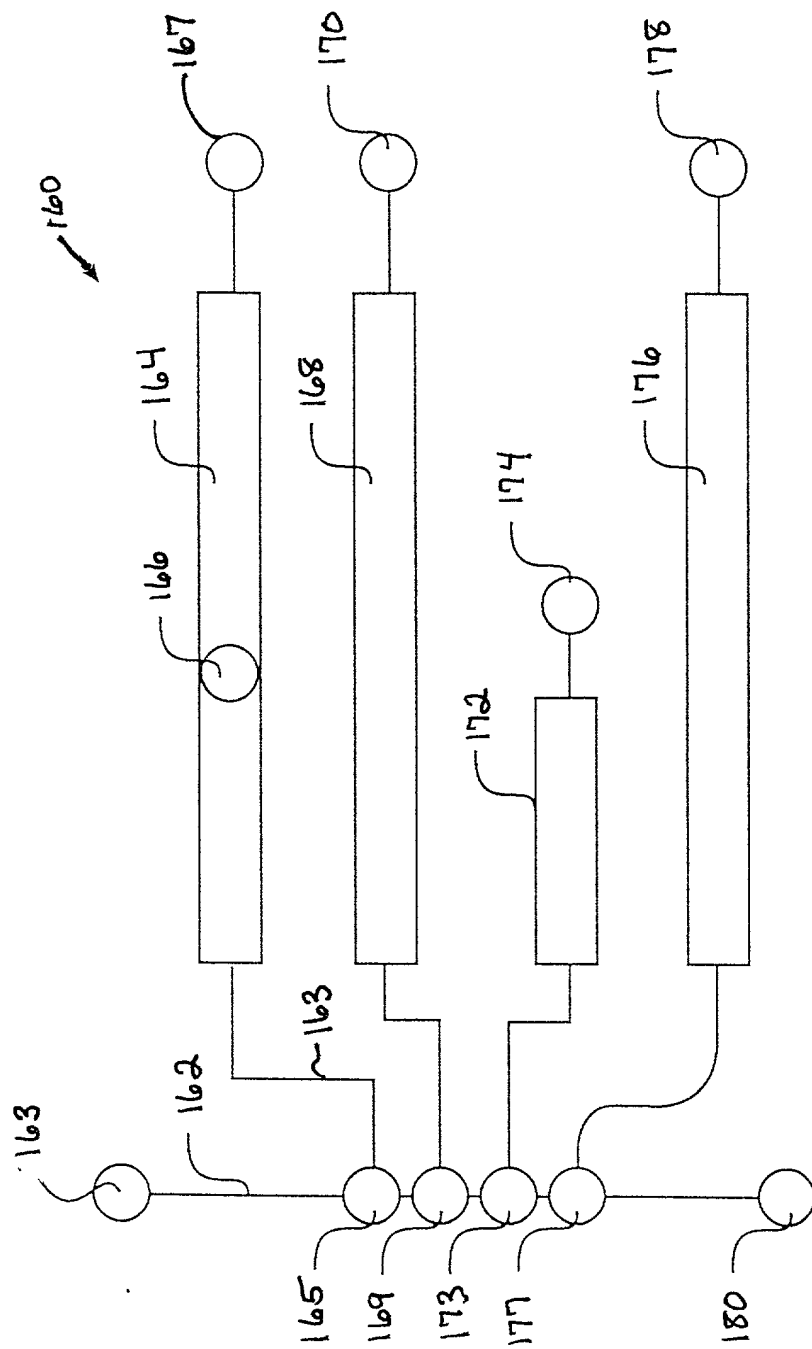
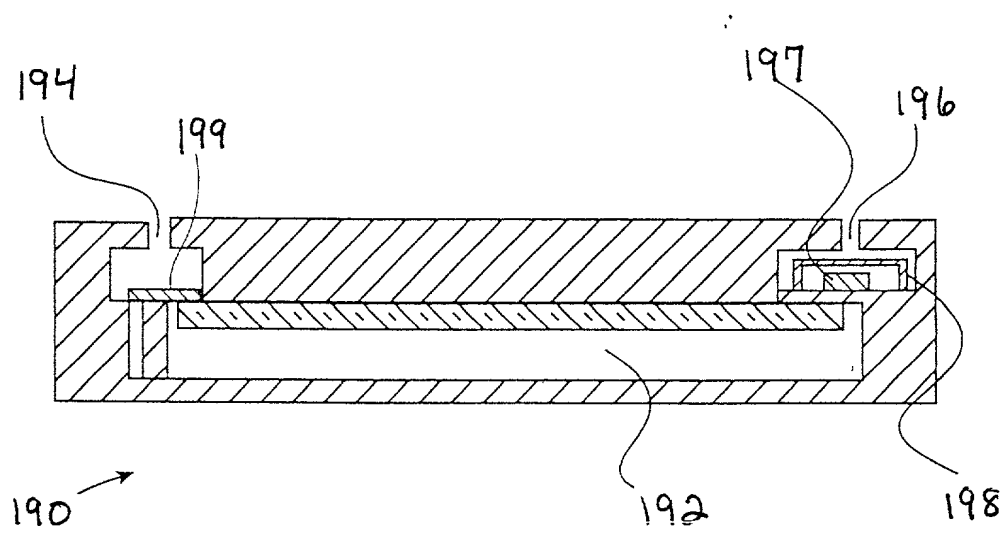
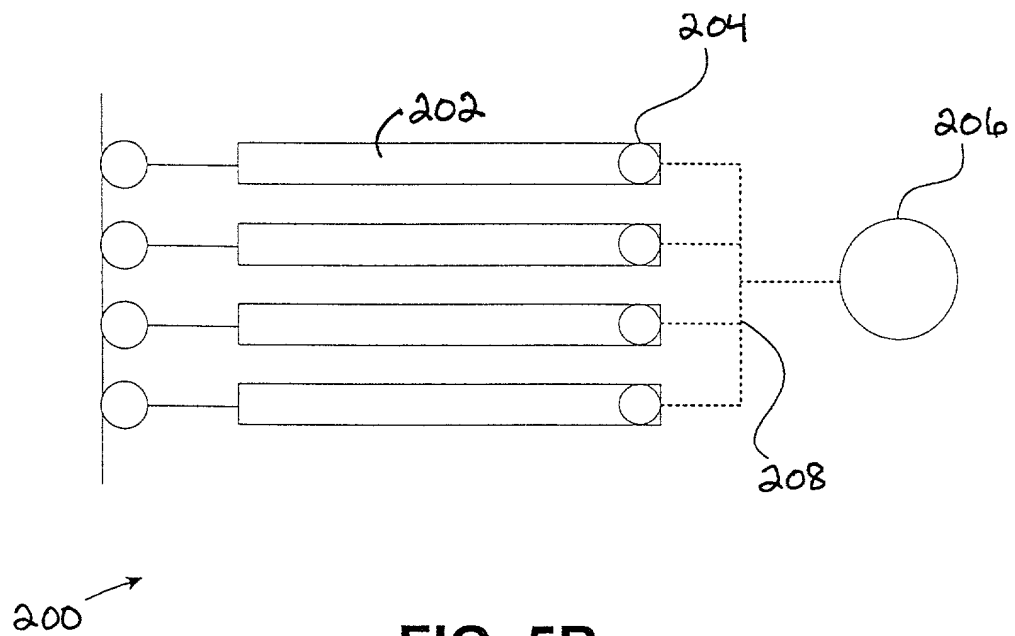


FIG. 5





**FIG.5A**



**FIG. 5B**



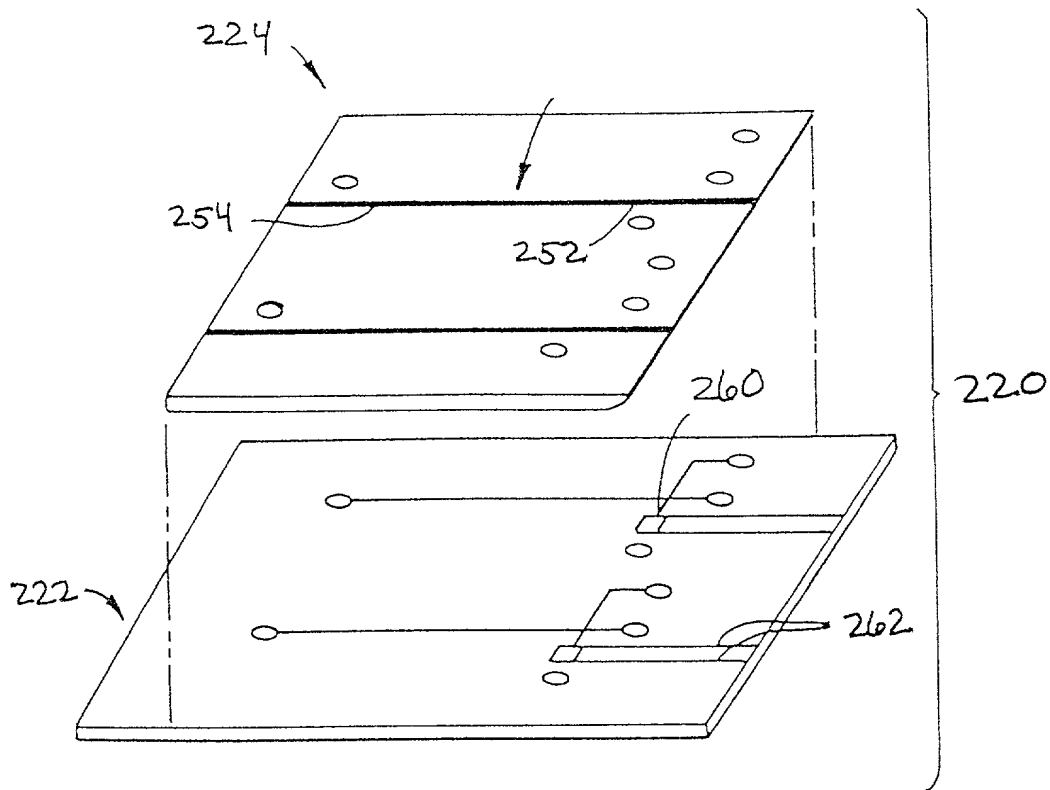
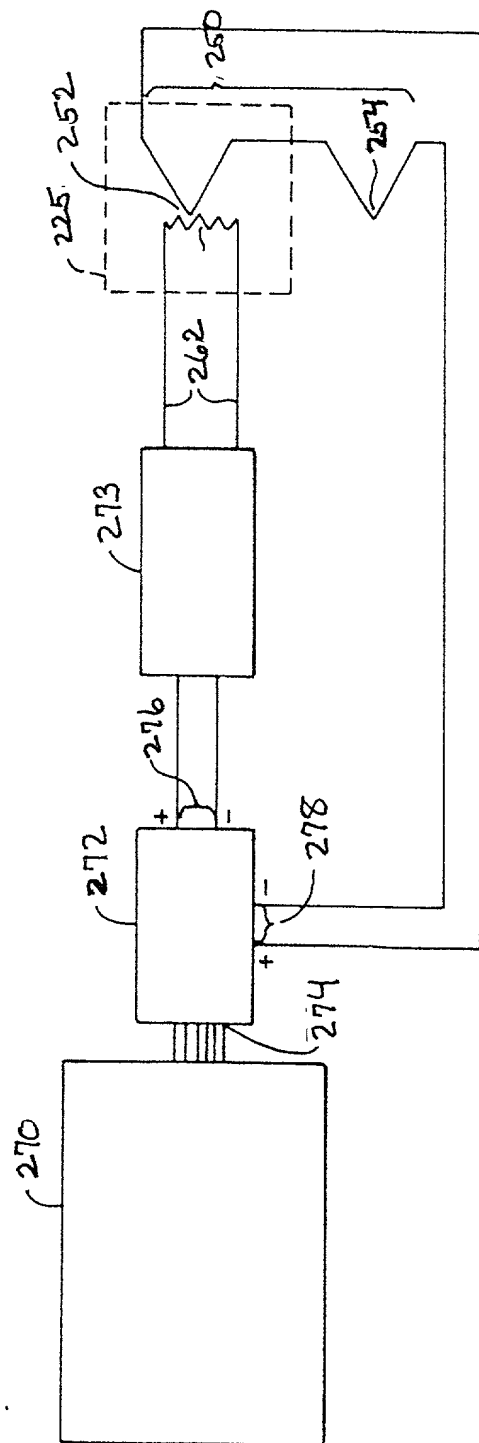
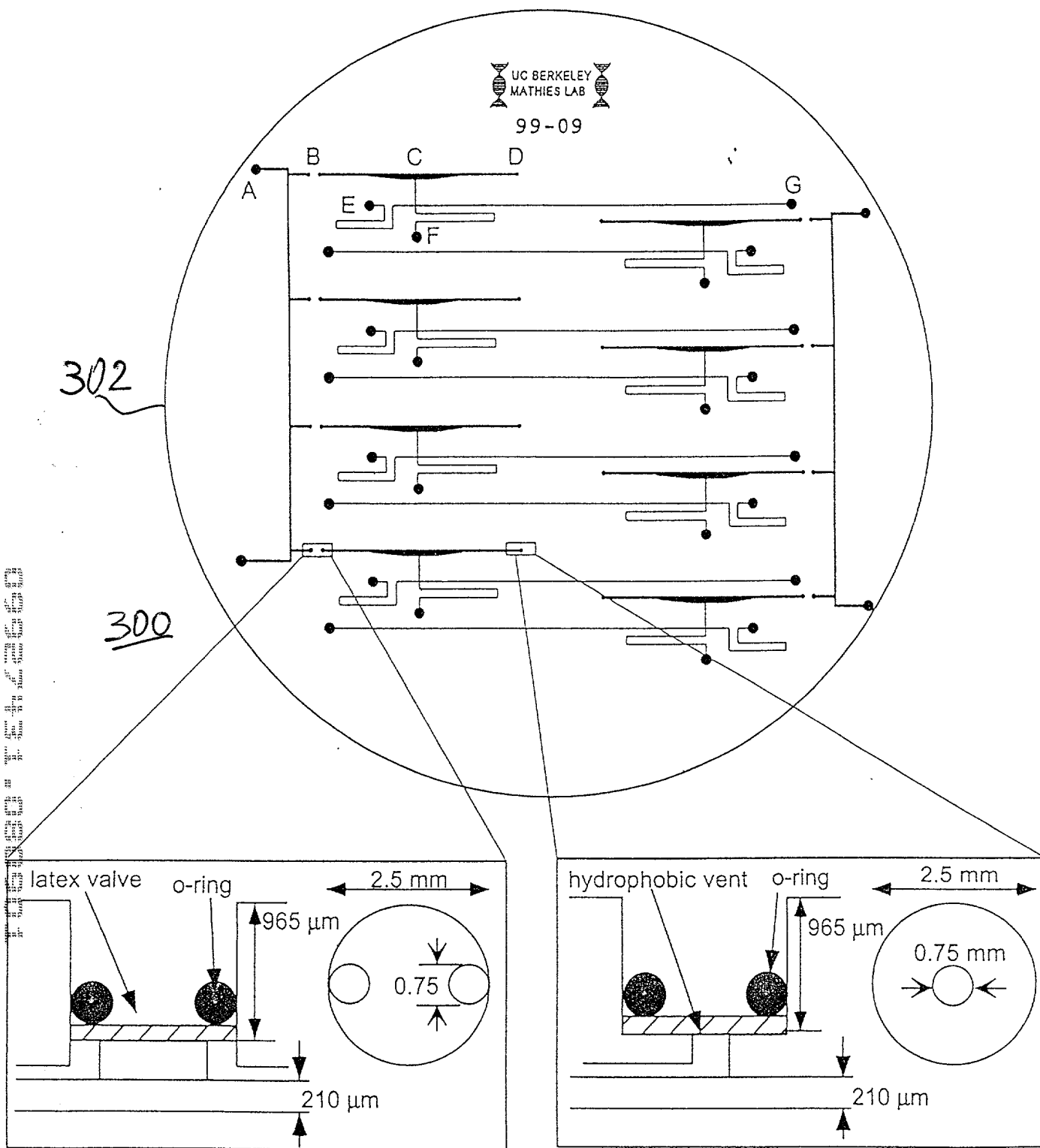


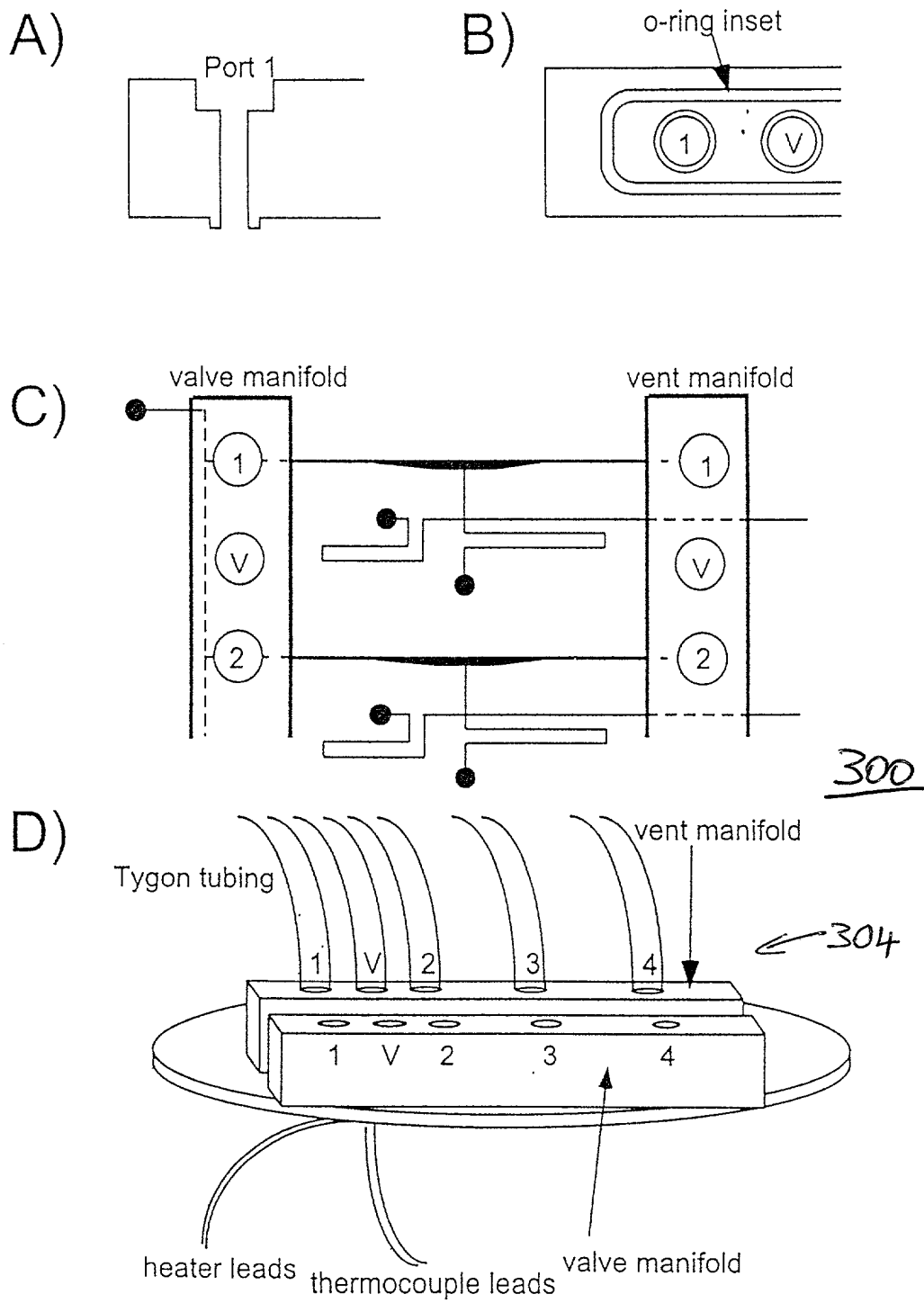
FIG. 6B



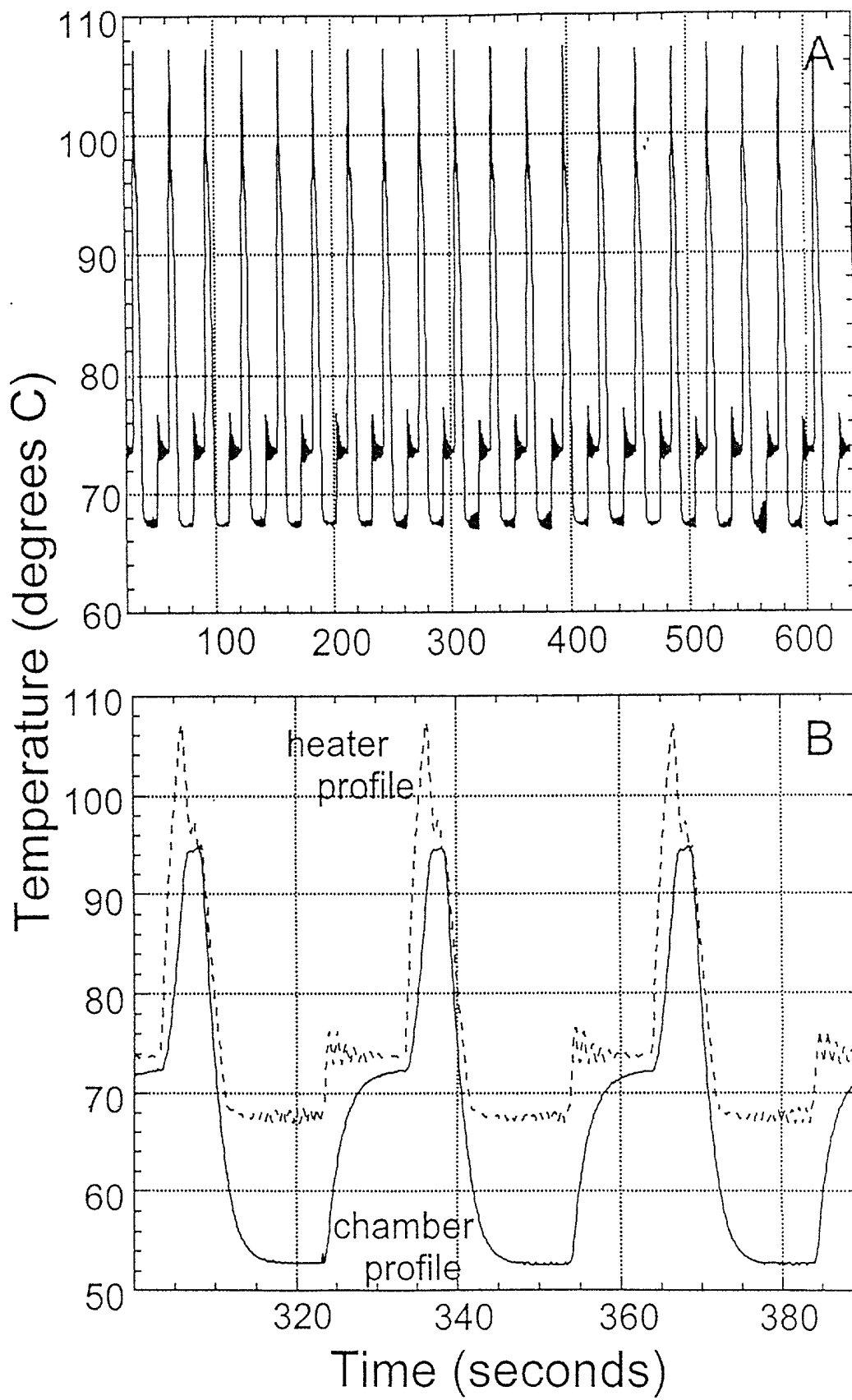
**FIG. 7**



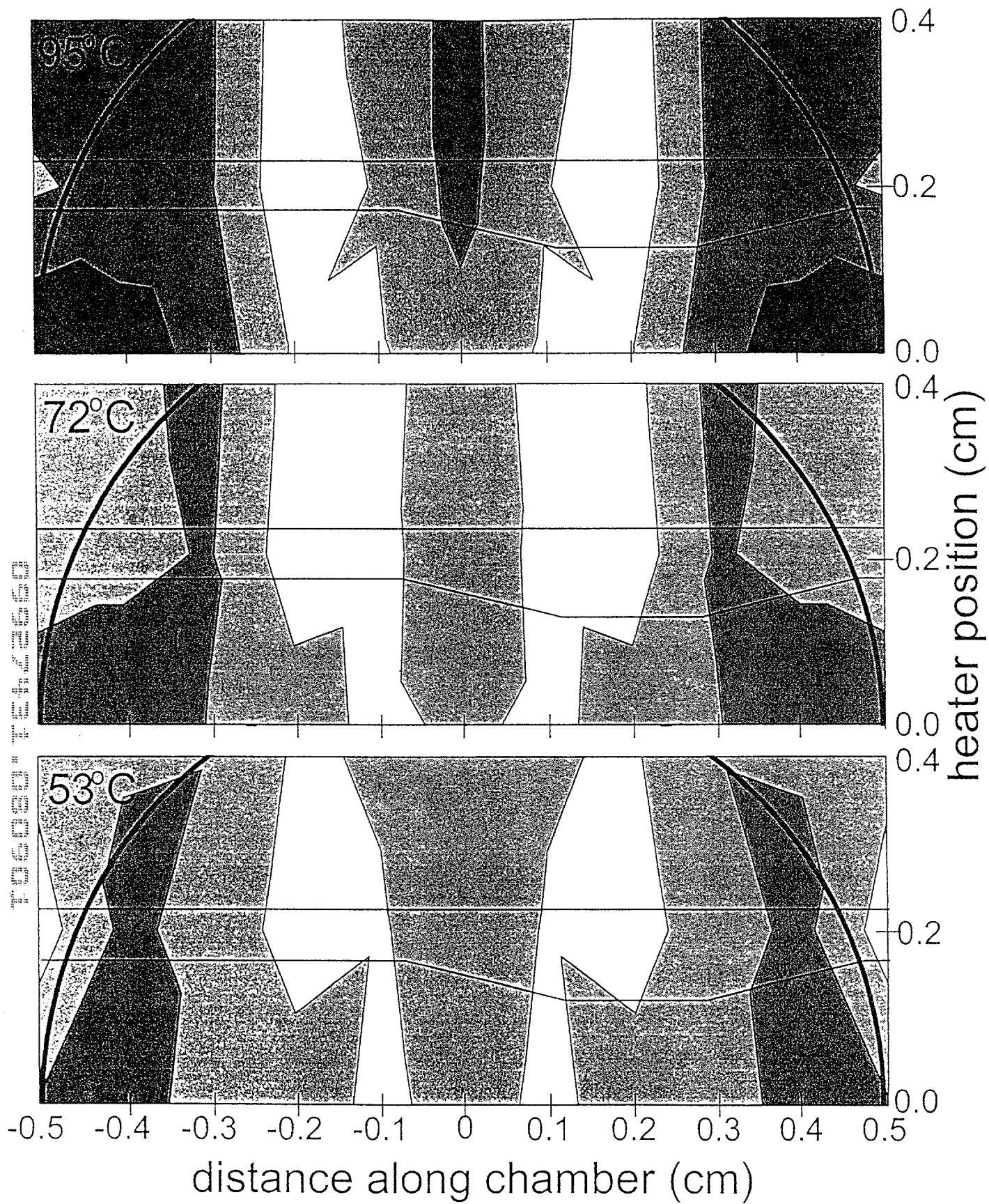
**FIG. 8**



**FIG. 9**

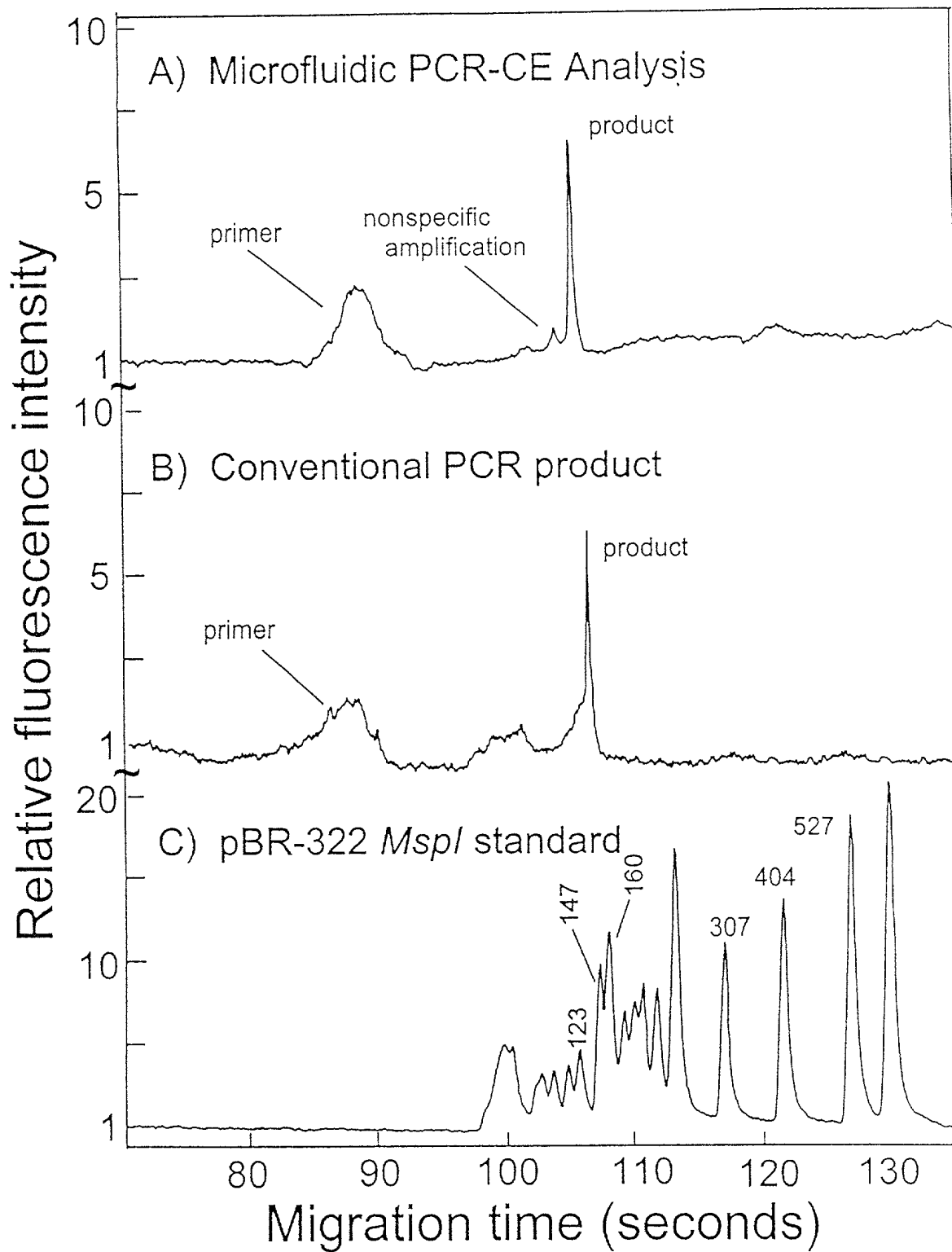


**FIG. 10**

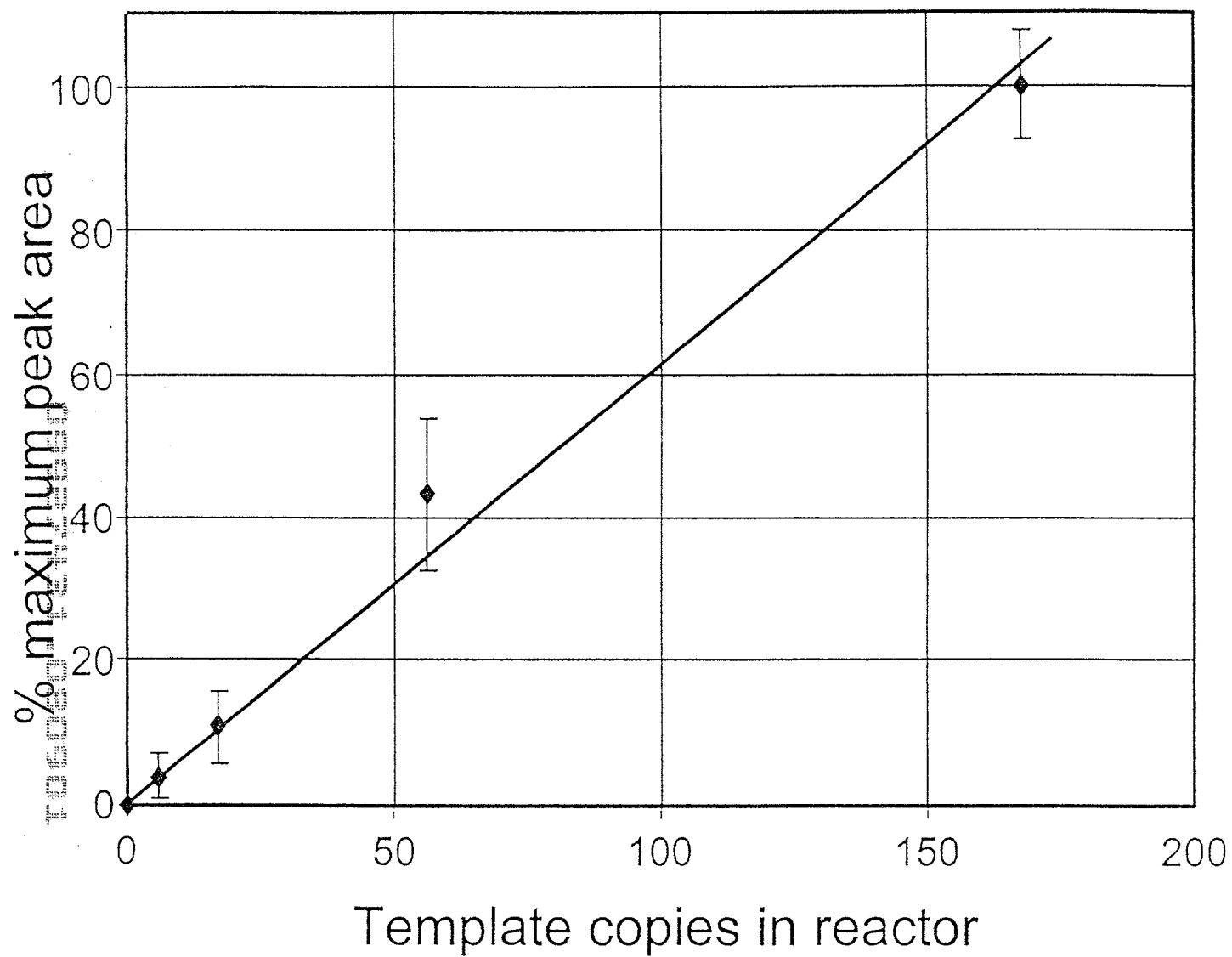


**FIG. 11**





**FIG. 12**



**FIG. 13**